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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Leonard Forbes

Title: SILICON-GERMANIUM DEVICES FOR CMOS FORMED BY ION IMPLANTATION AND SOLID PHASE EPITAXIAL REGROWTH

Attorney Docket No.: 303.229US2

PATENT APPLICATION TRANSMITTAL

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items and information (as indicated with an "X"):

X **DIVISIONAL** of prior Patent Application No. 08/717,198 (under 37 CFR § 1.53(b)) comprising:
- X Specification (11 pgs, including claims numbered 1 through 23 and a 1 page Abstract).
- X Formal Drawing(s) (2 sheets).
- X Copy of signed Combined Declaration and Power of Attorney (3 pgs) from prior application.
- X Associate Power of Attorney (1pg.)
- X Incorporation by Reference: *The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied herewith, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.*
- X Check in the amount of $790.00 to pay the filing fee.

X Prior application is assigned of record to Micron Technology, Inc. .

X Information Disclosure Statement (1 pgs), Form 1449 (1 pgs). References NOT enclosed, cited in prior application.

X Preliminary Amendment (1 pgs).

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The filing fee has been calculated below as follows:

	No. Filed	No. Extra	Rate	Fee
TOTAL CLAIMS	4 - 20 =	0	x 22 =	$0.00
INDEPENDENT CLAIMS	1 - 3 =	0	x 82 =	$0.00
[ ] MULTIPLE DEPENDENT CLAIMS PRESENTED				$0.00
BASIC FEE				$790.00
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By: _____
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By: Sheri Simms Signature: _____

S/N Unknown **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes	Examiner: Unknown
Serial No.:	Unknown	Group Art Unit: Unknown
Filed:	Herewith	Docket: 303.229US2
Title:	SILICON-GERMANIUM DEVICES FOR CMOS FORMED BY ION IMPLANTATION AND SOLID PHASE EPITAXIAL REGROWTH	

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

When the above-identified patent application is taken up for consideration, please amend the application as follows:

IN THE SPECIFICATION

On page 1, line 8, before "The present invention relates", please insert the sentence --This application is a division of U.S. Serial No. 08/717,198 filed September 18, 1996..--

IN THE CLAIMS

Please cancel claims 1-10 and 15-23 without prejudice.

REMARKS

Claims 1-10 and 15-23 are canceled, hereby, claims 11-14 are now pending in the application.

Respectfully submitted,

LEONARD FORBES

By their Representatives,

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Date 8/11/98 By _____
Edward J. Brooks, III
Reg. No. 40,925

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Name Signature

Silicon-Germanium Devices for CMOS Formed by Ion Implantation and Solid Phase Epitaxial Regrowth

Field of the Invention

The present invention relates to methods and apparatus for the manufacture of silicon-germanium semiconductor devices.

Background of the Invention

Complementary metal-oxide-semiconductor (CMOS) technology is widely used in integrated circuits (ICs) due to the lower power consumption of CMOS ICs, as compared to previously preferred NMOS ICs. CMOS is so named because it uses both p- and n-channel transistors in its ICs. However, one of the most fundamental and serious limitations of CMOS technology resides in the p-channel device. Generic, one-micron processes reflect such limitations in the disparate field-effect mobilities associated with n-channel and p-channel devices within a CMOS IC. In such devices, p-channel field-effect hole mobility is approximately two to three times lower than n-channel field-effect electron mobility. Thus, in order to achieve optimum symmetrical switching and driving capabilities, p-channel devices must be more than twice as large as n-channel devices, which undesirably affects packing density of an IC.

To overcome device-operational limitations in bipolar technology, as used in amplifying and switching devices, silicon-germanium ($Si_{1-x}Ge_x$)/Si heterojunctions were developed. $Si_{1-x}Ge_x$ has an associated band gap that is smaller than that of the silicon. When such a material is used for the emitter material in a bipolar transistor, a higher emitter-injection efficiency is obtained due to the bandgap difference between the silicon base material and the emitter material. To form a $Si_{1-x}Ge_x$/Si

heterojunction, molecular beam epitaxy (MBE) and ultrahigh-vacuum chemical vapor deposition (UHV CVD) are currently used.

It is desirable to adapt $Si_{1-x}Ge_x$/ Si heterojunction technology to improving field-effect mobilities of p-channel MOS devices used in CMOS ICs. However, while MBE and UHV CVD are two methods for forming a $Si_{1-x}Ge_x$/Si heterojunction, both techniques are not compatible with large-scale manufacturing processes, such as commonly used to form CMOS ICs. MBE and UHV CVD are complicated and expensive. MBE and UHV CVD were developed for use in fabricating bipolar devices, which are intolerable towards microdefects and dislocations resulting from strained layers, due to their extremely small base widths, which require very sharp profiles and transitions. It was not critical to develop an efficient, high volume technique for the fabrication of $Si_{1-x}Ge_x$ layers. Thus, it has not been possible to adapt $Si_{1-x}Ge_x$/Si heterojunction technology to the large volume manufacture of CMOS ICs. MOS devices are much more tolerant of microdefects and dislocations, since there is no concern about emitter-collector shorts resulting from the extremely small base widths inherent in bipolar devices.

Furthermore, conventional silicon CMOS transistor gates are formed by thermally oxidizing the silicon substrate. When a $Si_{1-x}Ge_x$ layer is formed on a silicon substrate, by MBE or UHV CVD, stable gate oxides can not be later formed on the $Si_{1-x}Ge_x$ layer. Oxides of Ge are not stable, thus, other ways of forming a gate oxide layer are being investigated. One way of forming a stable gate oxide over a $Si_{1-x}Ge_x$ layer is by depositing low temperature CVD oxides. However, such oxides have a resulting undesirable higher surface state density. Another way of forming a stable gate oxide over a $Si_{1-x}Ge_x$ layer is by reoxidation of a silicon cap layer applied over the $Si_{1-x}Ge_x$ layer. However, using a silicon cap layer results in a buried channel structure with an undesirably large effective gate oxide thickness. Furthermore, at high gate voltages, many of the $Si_{1-x}Ge_x$ layer carriers migrate to the silicon cap layer. The net result is a loss in device performance.

There is a need for a method of large volume manufacturing of Si-Ge semiconductor devices. In particular, there is a need for a method of large volume manufacturing of silicon-germanium CMOS ICs, in which a stable gate oxide layer can exist over a $Si_{1-x}Ge_x$ transistor channel.

Summary of the Invention

The present invention teaches a method and apparatus for large volume manufacturing of Si-Ge complementary metal-oxide-semiconductor (CMOS) integrated circuits (ICs). $Si_{1-x}Ge_x$ is formed under existing gate oxide layers, eliminating the problem of forming stable gate oxides directly over a $Si_{1-x}Ge_x$ layer. A high dose Ge layer is implanted under the gate oxide layer. Next, a $Si_{1-x}Ge_x$ layer is grown by solid phase epitaxial (SPE) regrowth, such that lattice mismatch is minimized between the $Si_{1-x}Ge_x$ layer and the underlying Si substrate. SPE is performed in a low temperature furnace, for approximately ten minutes. Implantation and anneal steps are commonplace in the large volume manufacture of CMOS ICs. Thus, this invention does not add significant cost or complexity to the manufacture of CMOS ICs, while providing the ability to manufacture high volume CMOS ICs with enhanced field effect hole mobility.

According to one aspect of the invention, the $Si_{1-x}Ge_x$ layer formed in this invention has a critical layer thickness, which depends on the molar fraction, x, of germanium present in the $Si_{1-x}Ge_x$ compound formed. As long as the critical layer thickness is not exceeded, $Si_{1-x}Ge_x$ will form defect-free during SPE regrowth. By forming p-channels in accordance with the method of the invention, valuable chip space is conserved, enabling high density chips to be formed. P-channel transistors are able to be formed in approximately the same amount of space as n-channel transistors due to the increased field effect hole mobility, while obtaining symmetrical switching and driving capabilities.

Brief Description of the Drawings

Figures 1A to 1C are cross-sectional representations of the method of forming Si-Ge CMOS ICs.

Figure 2 is a graphical representation of the critical thickness of a $Si_{1-x}Ge_x$ layer with respect to the molar fraction of germanium, x, present in the layer.

Description of the Embodiments

In the following detailed description, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that structural, logical and electrical changes may be made without departing from the spirit and scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims. Numbering in the Figures is usually done with the hundreds and thousands digits corresponding to the figure number, with the exception that the same components may appear in multiple figures.

In the manufacture of p-channel metal-oxide-semiconductor (PMOS), transistors for complementary metal-oxide-semiconductor (CMOS) integrated circuits (ICs) are formed, having $Si_{1-x}Ge_x$/Si heterojunctions. A $Si_{1-x}Ge_x$/Si heterojunction is formed between the substrate and the channel region. The presence of the heterojunction in each PMOS transistor substantially increases the speed of such devices due to an increase in the field-effect hole mobility. By increasing the speed of PMOS devices, they can be made smaller. Thus, chip density is improved.

The first steps in the manufacture of a PMOS transistor in accordance with the method of the invention are those used in the conventional manufacture of PMOS transistors, as shown in Figure 1A. These steps are: formation of active device

areas on a silicon substrate 110, defined by field oxide 112 and growth of a gate oxide layer 114 on the silicon substrate 110, as well known to one skilled in the art. The silicon substrate 112 is either a (n-) substrate or it comprises an (n-) well formed in a (p-) substrate.

Next, a $Si_{1-x}Ge_x$ channel is formed under the existing gate oxide layer 114, shown in Figure 1A, eliminating the problem of forming stable gate oxides directly over a $Si_{1-x}Ge_x$ layer. Using conventional photoresist masking and patterning techniques, all but the gate oxide layer 114 are protected from implantation with a photoresist layer 115. Then, a high dose (approximately 2×10^{16} atoms/cm^2) of Ge is implanted under the gate oxide layer 114. The Ge is implanted to a depth of between 100 to 1,000 angstroms, preferably approximately 300 angstroms, to form an implanted region 118 as shown in Figure 1B. The implant energy is less than 200 keV, preferably at an energy of approximately 20 to 100 keV, so as not to significantly damage the gate oxide layer 114. Subsequently, the photoresist layer 115 is removed.

Next, the $Si_{1-x}Ge_x$ layer 120 for the channel, as shown in Figure 1C, is grown by solid phase epitaxial (SPE) regrowth, such that lattice mismatch is minimized between the $Si_{1-x}Ge_x$ layer 120 and the underlying Si substrate 110. SPE is performed in a standard silicon processing low temperature furnace, for approximately ten minutes. The furnace temperature is approximately 450 to 700 degrees Celsius, preferably 550 degrees Celsius, to promote SPE regrowth.

A polysilicon gate 122 is then formed on the gate oxide layer 114, as shown in Figure 1C, and source/drain regions 116 are implanted, as well known to one skilled in the art. The resulting structure contains a $Si_{1-x}Ge_x$/Si heterojunction 124 between the channel 120 and the substrate 110. Due to the higher hole mobility in germanium, the field-effect hole mobility is increased significantly, contributing to faster PMOS transistors. Implantation and anneal steps are commonplace in the manufacture of CMOS ICs. Thus, this invention does not add significant cost or complexity to the manufacture of CMOS ICs.

The $Si_{1-x}Ge_x$ channel 120 formed in this invention has a thickness 128, as shown in Figure 1C and the critical values of which are represented by the graph in Figure 2. The critical thickness of the $Si_{1-x}Ge_x$ channel 120 depends on the molar fraction, x, of germanium present in the $Si_{1-x}Ge_x$ layer 120. As long as the critical layer thickness is not exceeded, $Si_{1-x}Ge_x$ 120 will form defect-free during SPE regrowth, as desired. The region 230 below and to the left of the plotted line in Figure 2 is the permissible range of $Si_{1-x}Ge_x$ channel thickness 128 with respect to the molar fraction, x, of germanium. For example, when the molar fraction, x, of germanium is approximately 0.2, as preferred, it is preferable to form a $Si_{1-x}Ge_x$ channel 120, having a thickness 128 of approximately 100 angstroms to 1,000 angstroms, while staying within the critical thickness range.

It is to be understood that the above description is intended to be illustrative, and not restrictive. Many other embodiments will be apparent to those of skill in the art upon reviewing the above description. The scope of the invention should, therefore, be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

What is claimed is:

1. A method for manufacturing a silicon/germanium semiconductor transistor on a silicon substrate, comprising the steps of:

forming a gate oxide on the substrate;

implanting germanium into the substrate, only beneath the gate oxide, to form an implanted region;

annealing the substrate to form $Si_{1-x}Ge_x$ in the implanted region, having a germanium molar fraction of x;

forming a gate on the gate oxide; and

forming source/drain regions in the substrate.

2. The method of claim 1, wherein the implanting step comprises implanting germanium at a dose of approximately 2×10^{16} atoms/cm^2.

3. The method of claim 1, wherein the implanting step comprises implanting germanium at an energy of approximately 20 to 100 keV.

4. The method of claim 1, wherein the implanting step comprises implanting germanium to a depth of approximately 100 to 1,000 angstroms.

5. The method of claim 1, wherein the implanting step comprises implanting germanium to a depth of approximately 300 angstroms.

6. The method of claim 1, wherein the annealing step comprises annealing in a furnace at a temperature of approximately 450 to 700 degrees Celsius.

7. The method of claim 1, wherein the annealing step comprises annealing in a furnace at a temperature of approximately 550 degrees Celsius.

8. The method of claim 1, wherein the $Si_{1-x}Ge_x$ formed is approximately 100 to 1,000 angstroms thick.

9. The method of claim 1, wherein the molar fraction of germanium is approximately 0.2.

10. The method of claim 1, wherein the silicon/germanium semiconductor transistor is a p-channel metal-oxide-semiconductor transistor.

11. A semiconductor transistor, comprising:

a silicon substrate;

a gate oxide, coupled to the substrate;

a gate, coupled to the gate oxide;

source/drain regions formed in the substrate on opposite sides of the gate; and

a $Si_{1-x}Ge_x$ channel region, having a germanium molar fraction of x, and formed in the substrate, underneath the gate oxide and between the source/drain regions.

12. The transistor of claim 11, wherein the transistor is a p-channel metal-oxide-semiconductor transistor.

13. The transistor of claim 11, wherein the $Si_{1-x}Ge_x$ channel is approximately 100 to 1,000 angstroms thick.

14. The transistor of claim 11, wherein the molar fraction of germanium is approximately 0.2.

15. A method for forming a p-channel in a metal-oxide-semiconductor transistor, comprising the steps of:

implanting germanium into the channel region of a transistor formed on a silicon substrate, through a gate oxide, to form an implanted region; and

annealing the implanted region to form $Si_{1-x}Ge_x$ in the channel region, having a molar fraction of germanium, x.

16. The method of claim 15, wherein the implanting step comprises implanting germanium at a dose of approximately 2×10^{16} atoms/cm^2.

17. The method of claim 15, wherein the implanting step comprises implanting germanium at an energy of approximately 20 to 100 keV.

18. The method of claim 15, wherein the implanting step comprises implanting germanium to a depth of approximately 100 to 1,000 angstroms.

19. The method of claim 15, wherein the implanting step comprises implanting germanium to a depth of approximately 300 angstroms.

20. The method of claim 15, wherein the annealing step comprises annealing in a furnace at a temperature of approximately 450 to 700 degrees Celsius.

21. The method of claim 15, wherein the annealing step comprises annealing in a furnace at a temperature of approximately 550 degrees Celsius.

22. The method of claim 15, wherein the $Si_{1-x}Ge_x$ channel is approximately 100 to 1,000 angstroms thick.

23. The method of claim 15, wherein the molar fraction of germanium is approximately 0.2.

Abstract of the Disclosure

A PMOS transistor is formed in a CMOS integrated circuit, having a $Si_{1-x}Ge_x/Si$ heterojunction between the channel region and the substrate. The method is applicable to large volume CMOS IC fabrication. Germanium is implanted into a silicon substrate, through a gate oxide layer. The substrate is then annealed in a low temperature furnace, to form $Si_{1-x}Ge_x$ in the channel region.

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JENNIFER HOFF
(Name)

Jennifer Hoff 9-18-96
(Signature) (date)

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Printed Name: Sher. Simms
Signature: Sher Simms

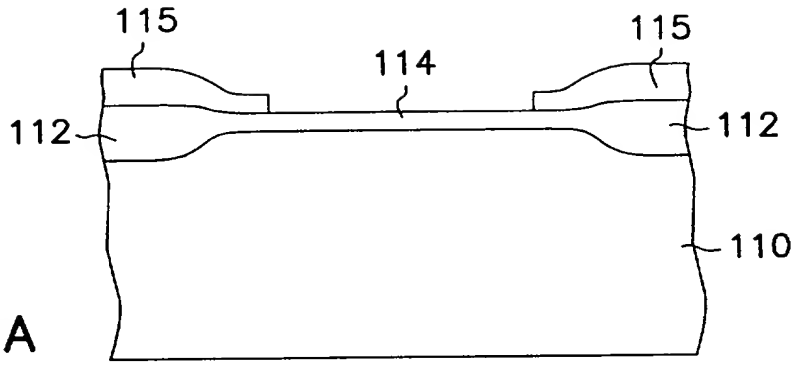

FIG. 1A

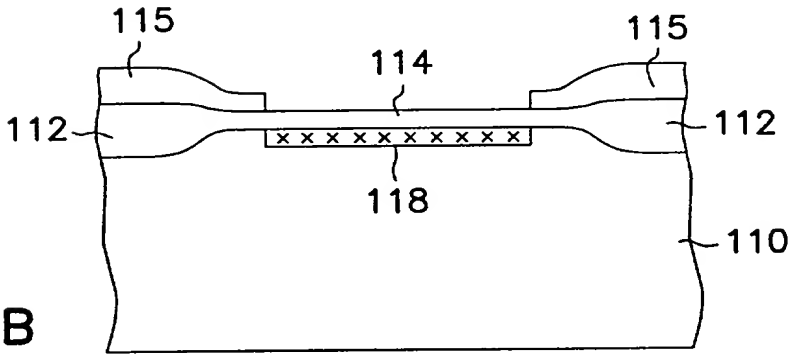

FIG. 1B

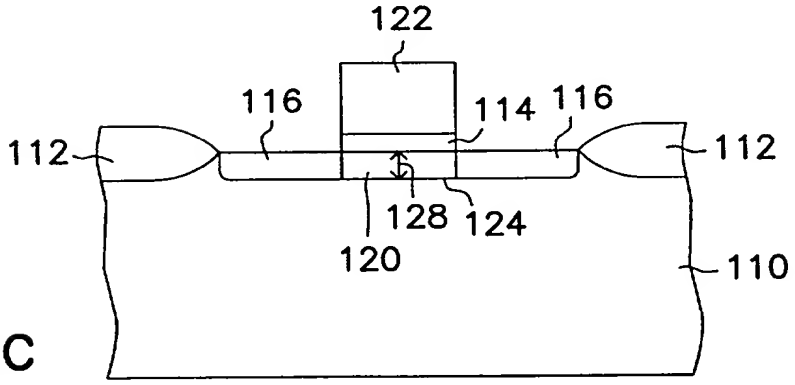

FIG. 1C

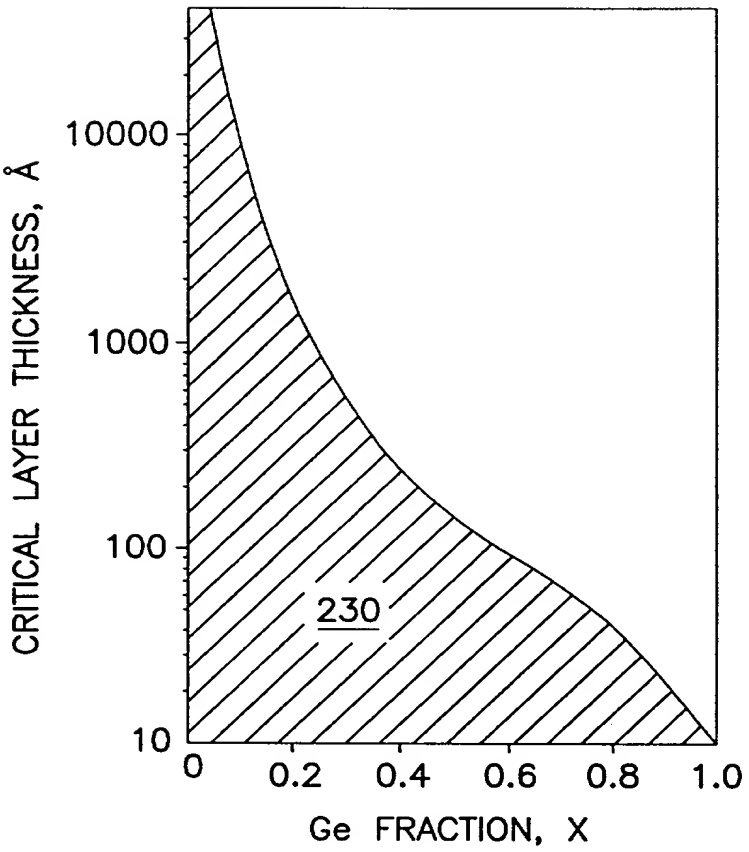
CRITICAL LAYER THICKNESS, Å
10000
1000
100
10
230
0
0.2
0.4
0.6
0.8
1.0
Ge FRACTION, X

FIG. 2

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: **SILICON-GERMANIUM DEVICES FOR CMOS FORMED BY ION IMPLANTATION AND SOLID PHASE EPITAXIAL REGROWTH**.

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (see page 3 attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, §119/365 of any foreign application(s) for patent of inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

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I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

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I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

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I hereby appoint the following attorney(s) and/or patent agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

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Dryja, Michael A.	Reg. No. 39,662	Kluth, Daniel J.	Reg. No. 32,146	Viksnins, Ann S.	Reg. No. 37,748
Embretson, Janet E.	Reg. No. 39,665	Lemaire, Charles A.	Reg. No. 36,198	Woessner, Warren D.	Reg. No. 30,440
Farney, W. Bryan	Reg. No. 32,651	Lempia, Bryan J.	Reg. No. 39,746		

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Telephone No. (612)339-0331

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of sole inventor : **Leonard Forbes**
Citizenship: **United States of America** Residence: **Corvallis, OR**
Post Office Address: 965 NW Highland Terrace
Corvallis, OR 97330

Signature: _____ Date: 12 SEPT 96
Leonard Forbes

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

Signature: _____ Date: _____

Full Name of inventor:
Citizenship: Residence:
Post Office Address:

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§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

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(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

S/N Unknown **PATENT**

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Applicant:	Leonard Forbes	Examiner: Unknown
Serial No.:	Unknown	Group Art Unit: Unknown
Filed:	Herewith	Docket: 303.229US2
Title:	SILICON-GERMANIUM DEVICES FOR CMOS FORMED BY ION IMPLANTATION AND SOLID PHASE EPITAXIAL REGROWTH	

APPOINTMENT OF ASSOCIATE REPRESENTATIVE

Assistant Commissioner for Patents
Washington, D.C. 20231

The undersigned attorney of record in the above-identified patent application hereby appoints:

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to act as an associate attorney, and empowers the associate attorney to receive all correspondence from the U. S. Patent and Trademark Office, to amend the specification and drawings, to prosecute the application; and ratifies any act done by the associate in respect of the application.

Respectfully submitted,

LEONARD FORBES

By their Representatives,

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Date Aug. 11, 1998 By Daniel J. Kluth

Daniel J. Kluth
Reg. No. 32,146

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